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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
08/890,894	07/10/97	CHAUVEL G	TIF-15767A

LM02/0623
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EXAMINER	
TRAN, D	
ART UNIT	**PAPER NUMBER**
2752	6

DATE MAILED: 06/23/99

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary

Application No.	Applic[illegible]s)
08/890,894	Chauvel et al.
Examiner	**Group Art Unit**
Denise Tran	2752

☒ Responsive to communication(s) filed on *Apr 26, 1999* .

☐ This action is **FINAL.**

☐ Since this application is in condition for allowance except for formal matters, **prosecution as to the merits is closed** in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

A shortened statutory period for response to this action is set to expire *three* month(s), or thirty days, whichever is longer, from the mailing date of this communication. Failure to respond within the period for response will cause the application to become abandoned. (35 U.S.C. § 133). Extensions of time may be obtained under the provisions of 37 CFR 1.136(a).

Disposition of Claims

☒ Claim(s) *6-33* is/are pending in the application.

Of the above, claim(s) *26-33* is/are withdrawn from consideration.

☐ Claim(s) _____ is/are allowed.

☒ Claim(s) *6-25* is/are rejected.

☐ Claim(s) _____ is/are objected to.

☐ Claims _____ are subject to restriction or election requirement.

Application Papers

☒ See the attached Notice of Draftsperson's Patent Drawing Review, PTO-948.

☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

☐ The proposed drawing correction, filed on _____ is ☐approved ☐disapproved.

☐ The specification is objected to by the Examiner.

☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

☒ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

☒ All ☐ Some* ☐ None of the CERTIFIED copies of the priority documents have been

☐ received.

☒ received in Application No. (Series Code/Serial Number) *07/902,191* .

☐ received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

*Certified copies not received: _____ .

☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

☒ Notice of References Cited, PTO-892

☒ Information Disclosure Statement(s), PTO-1449, Paper No(s). *3*

☐ Interview Summary, PTO-413

☒ Notice of Draftsperson's Patent Drawing Review, PTO-948

☐ Notice of Informal Patent Application, PTO-152

--- SEE OFFICE ACTION ON THE FOLLOWING PAGES ---

Detailed Action

1. Claims 26-33 are withdrawn from further consideration by the examiner, 37 CFR 1.142(b) as being drawn to a non-elected invention. Election was made **without** traverse in Paper No. 6. Applicant's election without traverse of claims 6-25 in Paper No. 6 is acknowledged. Claims 6-25 are presented for examination.

2. The drawings are objected to because figs. 1, 2, 5, 7, 8, 13, and 16-17, the boxes should be labeled with appropriate descriptive matter. For example, box 14 of fig.5 should be labeled as "RAM memory". Correction is required.

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 12, 18 and 19 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

As per claim 19 recites the limitation "said protocol processor" in lines 1-2 and 5-6. There is insufficient antecedent basis for this limitation in the claim.

5. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

6. Claim 12 is rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. The current application fails to teach the local memory being a ROM, claim 12.

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 6-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Asano et al. (5,237,686) (hereinafter Asano).

As per claims 6, 9-14, 17, 20, 21, 23 and 24, Asano shows the use of an apparatus, comprising:

a first DSP module comprising a core, a program ROM and a local RAM (e.g. figure

1, element 11a and figure 2, elements 3, 22, 23);

a second module comprising a core, a program memory, and a ROM or RAM (e.g. figure 1, element 11b and figure 2, elements 3,17, 22, 23);

a synchronizing circuit for coupling the core of the first module to the core of the second module, which ensures only one of modules access to the memory circuit (e.g. figure 1, element 7); and

a memory circuit for coupling the local memory of the first module to the local memory of the second module (e.g. figure 1, element 10a).

Asano does not specifically show the modules as a processor. "Official Notice" is taken that both the concept and advantages of providing for the incorporation of a module into a processor is well known and expected in the art. It would have been obvious to one of ordinary skill in the art at the time the invention was made to include the incorporation of a module into a processor to Asano because it would provide for a reduction in chip space and signal lines between functional elements, leading to an increase in processing performance.

As per claim 7, Asano does not specifically show the use of the first processor being the main processor. "Official Notice" is taken that both the concept and advantages of providing for a main processor is well known and expected in the art. It would have been obvious to one of ordinary skill in the art to include a main processor to Asano because it would provide for one of the plurality of DSPs (i.e., main processor) to perform management functions necessary to keep the system operating.

As per claim 8, Asano does not specifically show the modules as a microprocessor.

"Official Notice" is taken that both the concept and advantages of providing for the incorporation of a module into a microprocessor is well known and expected in the art. It would have been obvious to one of ordinary skill in the art at the time the invention was made to include the incorporation of a module into a microprocessor to Asano because it would provide for a reduction in chip space and signal lines between functional elements, leading to an increase in processing performance.

As per claim 15, Asano shows the use of a DP memory (e.g. figure 1, element 10a) but does not specifically show the use of the memory being a RAM. "Official Notice" is taken that both the concept and advantages of providing for a memory as RAM is well known and expected in the art. It would have been obvious to one of ordinary skill in the art to include RAM to Asano because it would allow storage locations being accessed in any order of data thereby increasing speed of memory accessing.

As per claim 16, Asano does not specifically show the second processor as a protocol processor. "Official Notice" is taken that both the concept and advantages of providing for DSP to perform the function of processing protocols is well known and expected in the art. It would have been obvious to one of ordinary skill in the art to include protocol processing to Asano because it would Asano to perform protocol processing at a faster speed, while allowing networking communications using existing standards.

As per claim 18, Asano shows the use of the ROM (e.g. figure 2, element 23) but does not specifically show an incremental register connected to it. "Official Notice" is taken that both the concept and advantages of providing for a program counter is well known and

expected in the art. It would have been obvious to one of ordinary skill in the art to include a program counter to Asano because it would provide for a program having a sequence of instructions to be performed in the required sequence.

As per claim 19, Asano shows the use of the DSPs performing computation, read and write and completion operations (e.g. cols. 10-11), but does not specifically show an instruction set. "Official Notice" is taken that both the concept and advantages of providing for an instruction set is well known and expected in the art. It would have been obvious to one of ordinary skill in the art to include an instruction set for each DSP to Asano because it would provide for the instruction which was decoded to be performed.

As per claims 22 and 25, Asano does not specifically show the memory circuit as part of the first processor. "Official Notice" is taken that both the concept and advantages of providing for a memory within a processor is well known and expected in the art. It would have been obvious to one of ordinary skill in the art at the time the invention was made to include the incorporation of a memory into a processor to Asano because it would provide for a reduction in chip space and signal lines between functional elements, leading to an increase in processing performance.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Denise Tran whose telephone number is (703) 305-9823. The examiner can normally be reached on Monday and Thursday from 8.30 to 6.00 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's

supervisor, John Cabeca, can be reached on (703) 308-3116. The fax phone number for the organization where this application or proceeding is assigned is (703) 305-9731.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-9600.

Denise Tran

06/17/99

JOHN W. CABECA
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